FIG.1

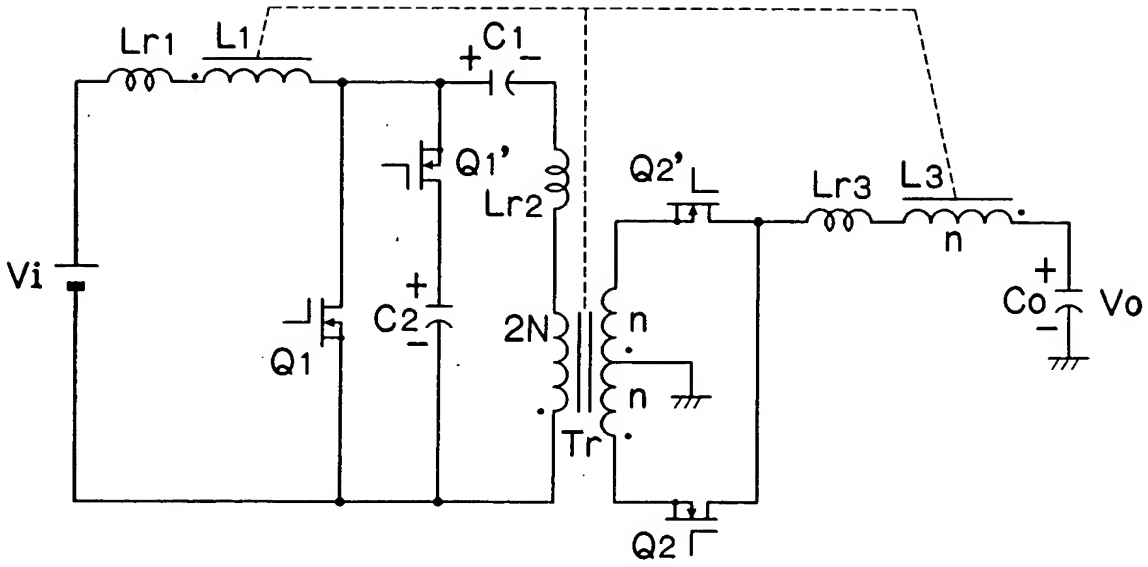


FIG.2

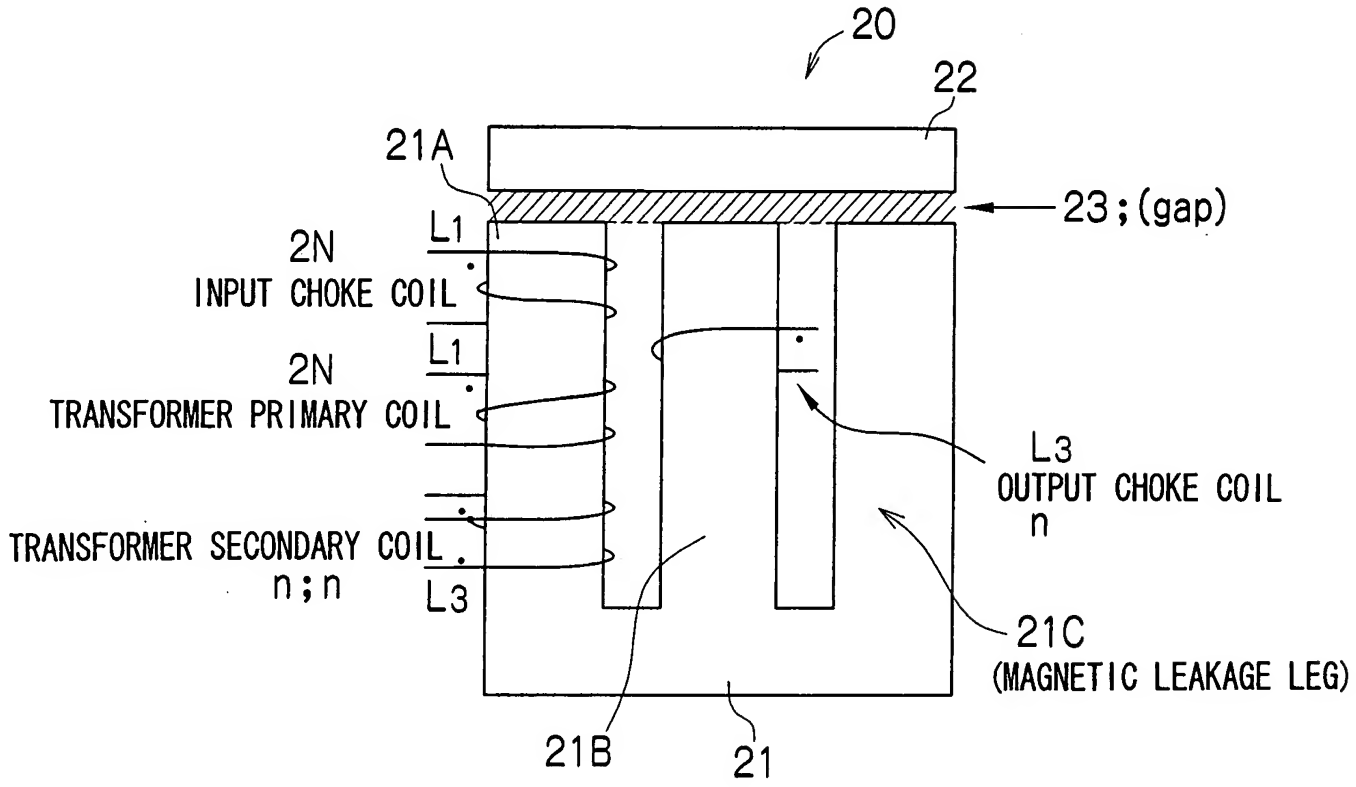

20
22
21A
23;(gap)
L1
2N
INPUT CHOKE COIL
L1
2N
TRANSFORMER PRIMARY COIL
L3
OUTPUT CHOKE COIL
n
TRANSFORMER SECONDARY COIL
n;n
L3
21C
(MAGNETIC LEAKAGE LEG)
21B
21

FIG.3

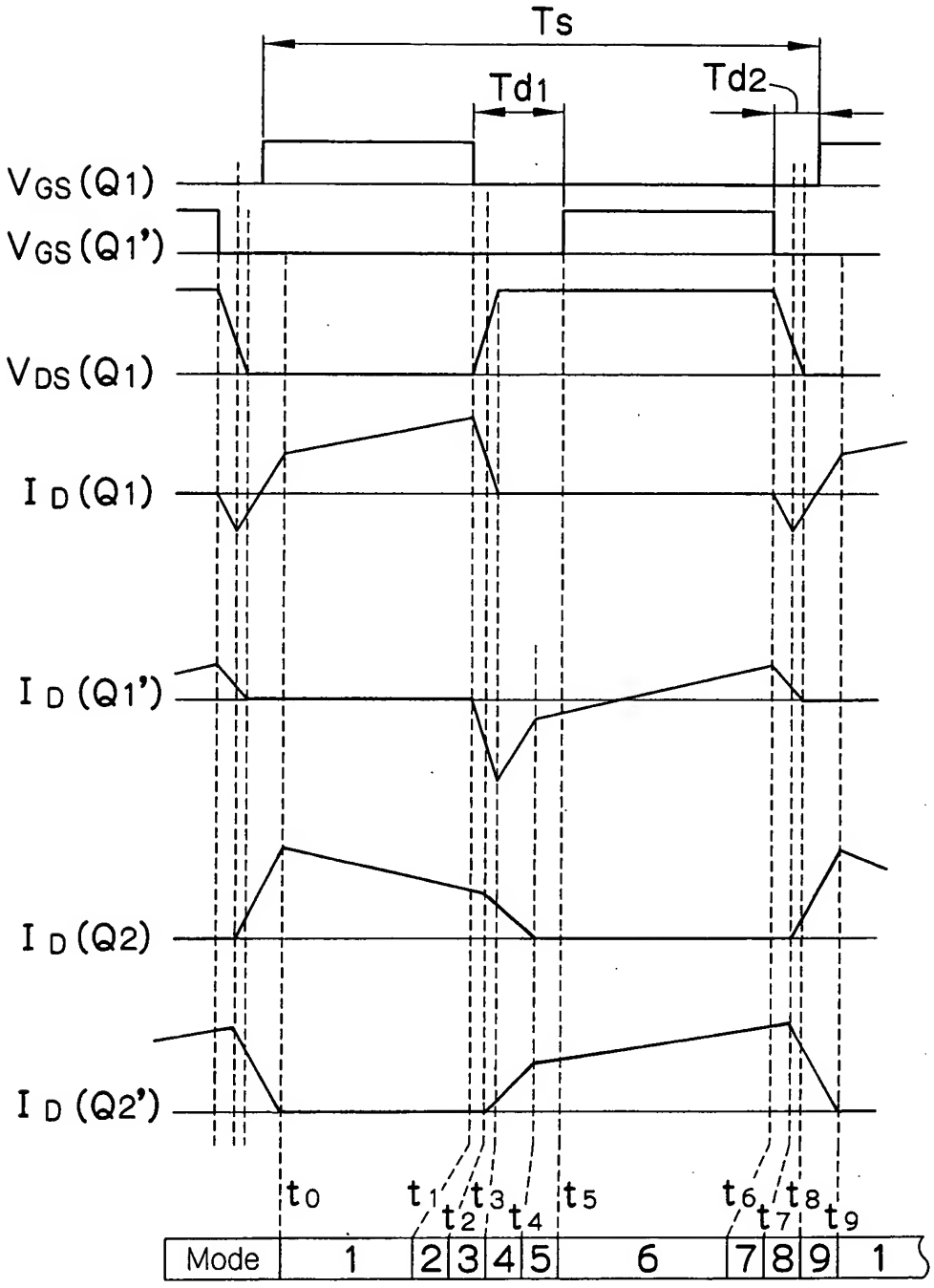

Ts
Td1
Td2
VGS(Q1)
VGS(Q1')
VDS(Q1)
ID(Q1)
ID(Q1')
ID(Q2)
ID(Q2')
t0
t1
t2
t3
t4
t5
t6
t7
t8
t9
Mode
1
2
3
4
5
6
7
8
9
1

FIG.4

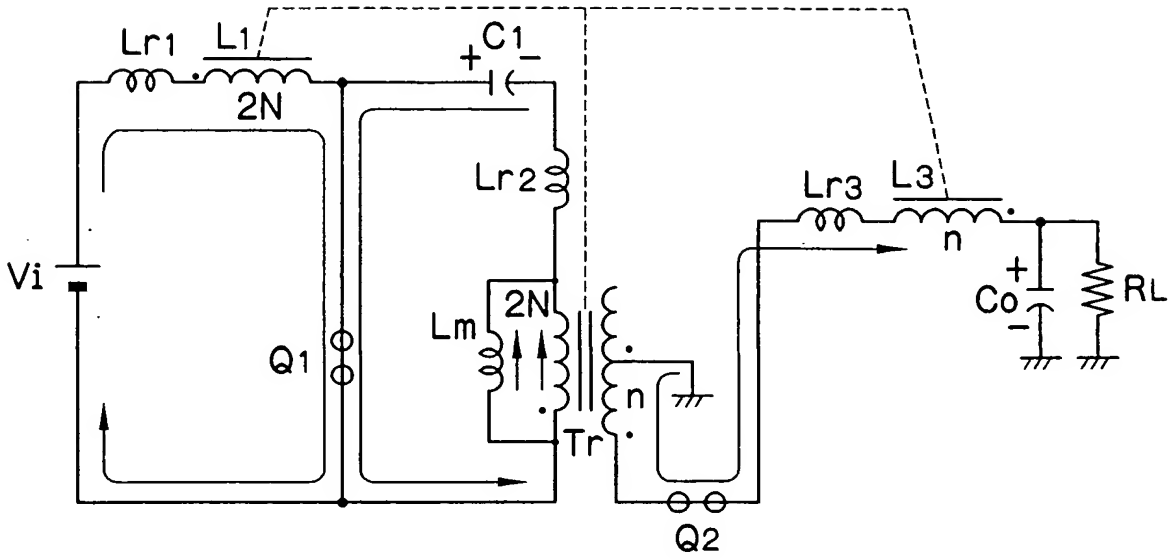

MODE 1
Lr1
L1
2N
C1
Lr2
Lr3
L3
n
Vi
Q1
Lm
2N
n
Tr
Co
RL
Q2

FIG.5

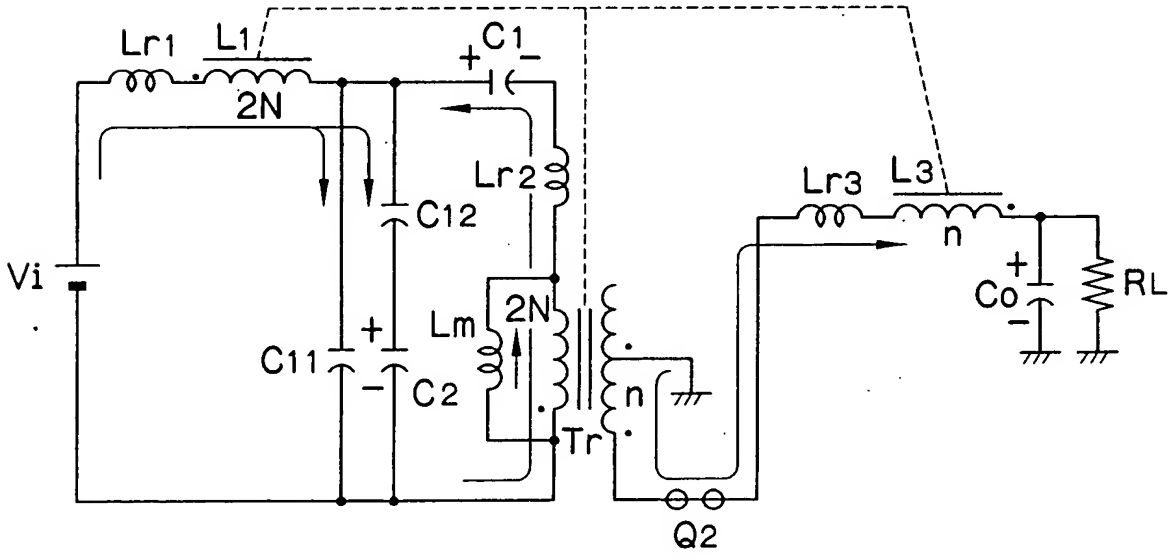

MODE 2
Lr1
L1
2N
C1
Lr2
Lr3
L3
n
C12
Vi
C11
C2
Lm
2N
n
Tr
Co
RL
Q2

FIG.6

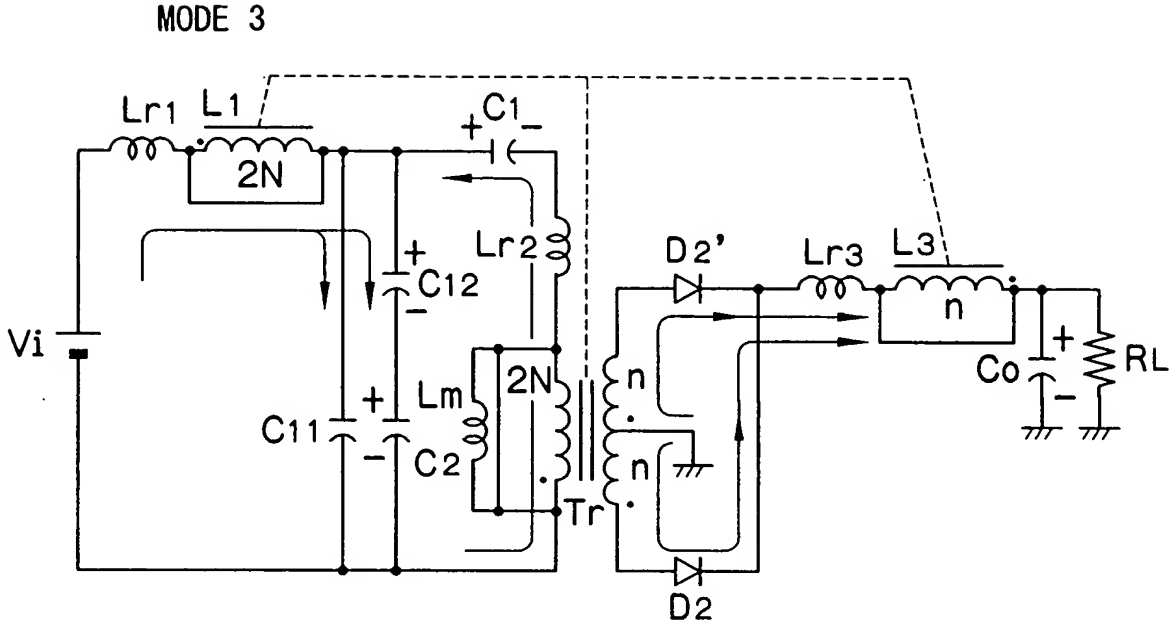

MODE 3
Lr1
L1
2N
C1
Lr2
D2'
Lr3
L3
n
C12
Vi
Lm
2N
n
Co
RL
C11
C2
n
Tr
D2

FIG.7

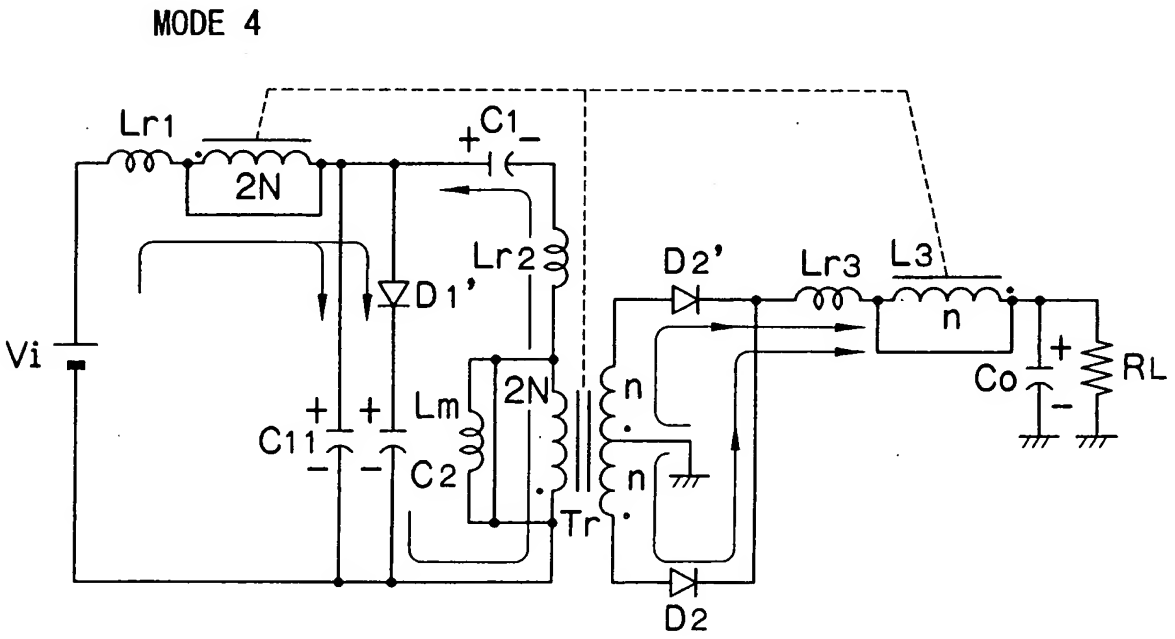

MODE 4
Lr1
2N
C1
Lr2
D2'
Lr3
L3
n
D1'
Vi
Lm
2N
n
Co
RL
C11
C2
n
Tr
D2

FIG.8

MODE 5

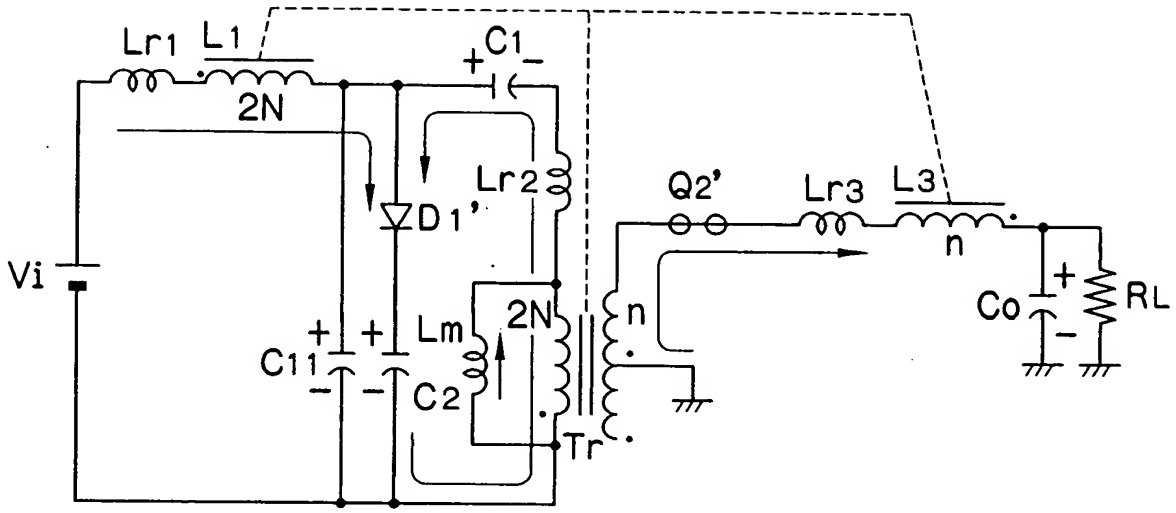


FIG.9

MODE 6

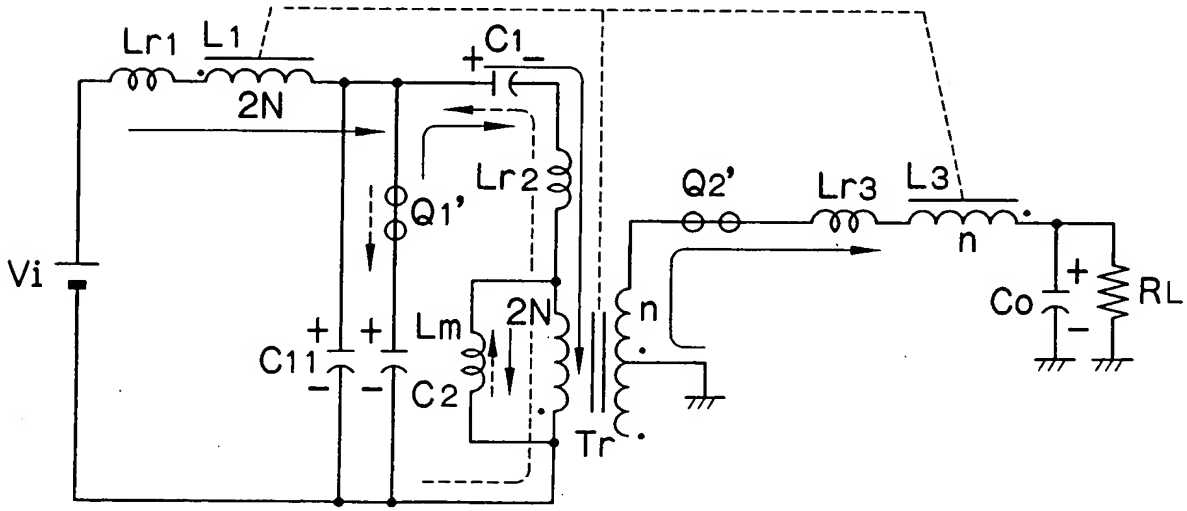


FIG.10

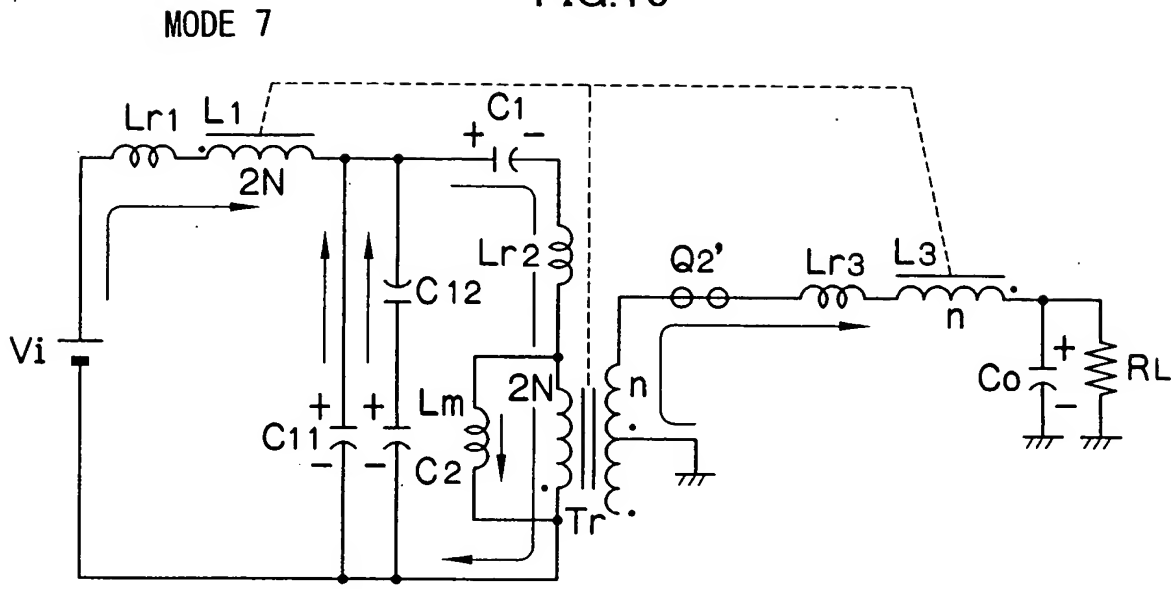

MODE 7
Lr1
L1
2N
C1
Lr2
C12
Q2'
Lr3
L3
n
Vi
Lm
2N
n
Co
RL
C11
C2
Tr

FIG.11

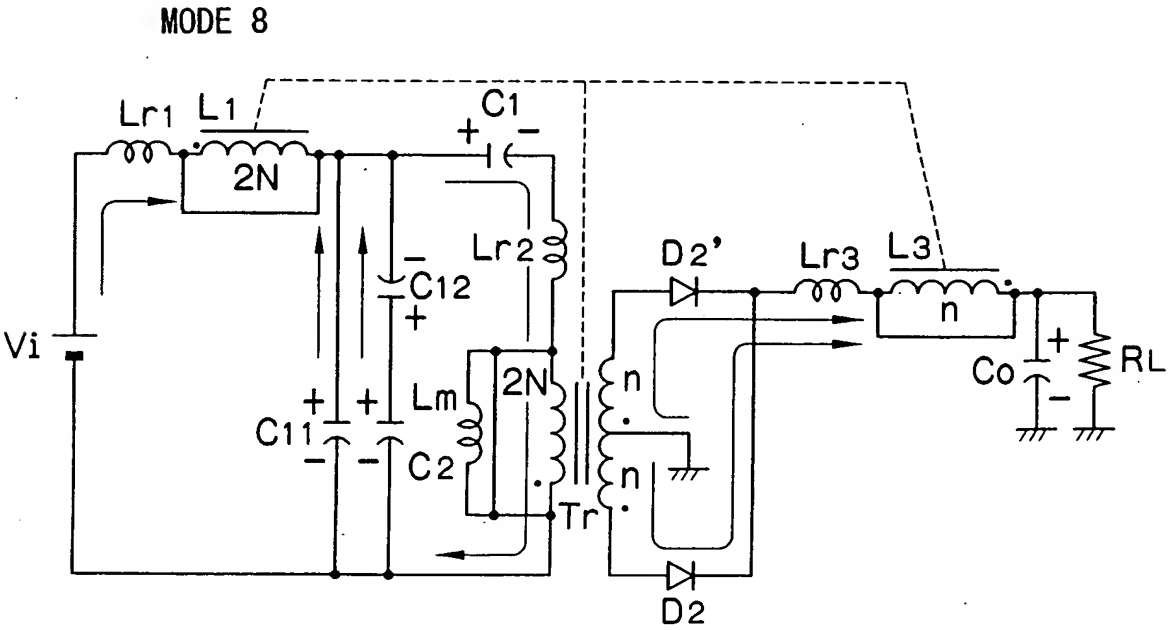

MODE 8
Lr1
L1
2N
C1
Lr2
C12
D2'
Lr3
L3
n
Vi
Lm
2N
n
Co
RL
C11
C2
Tr
D2

FIG.12

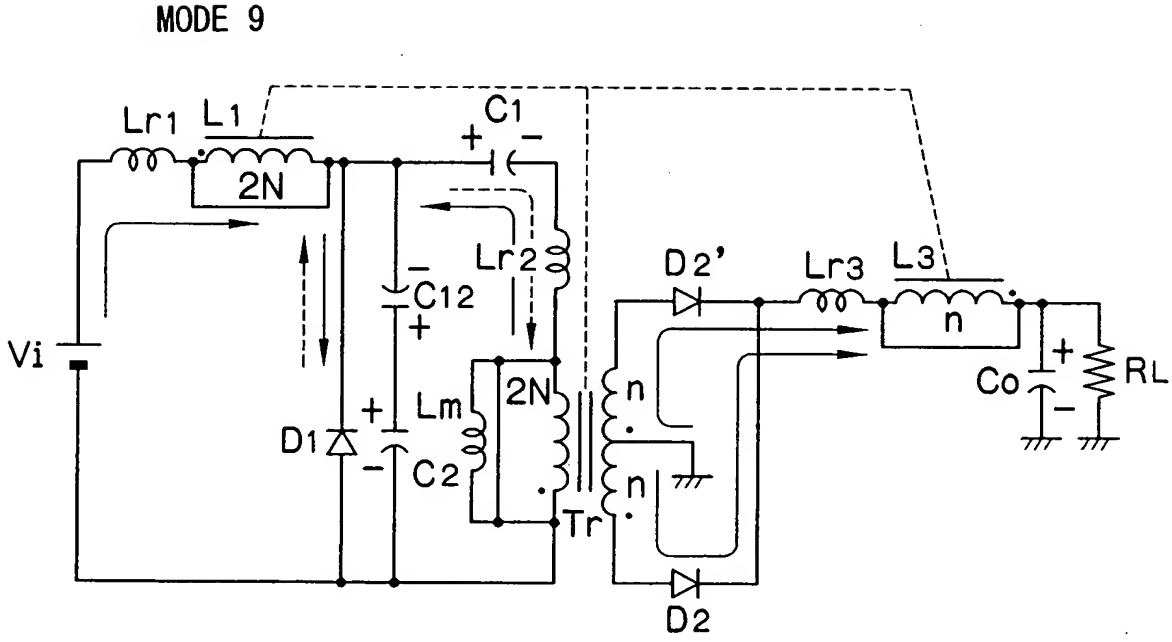


FIG.13

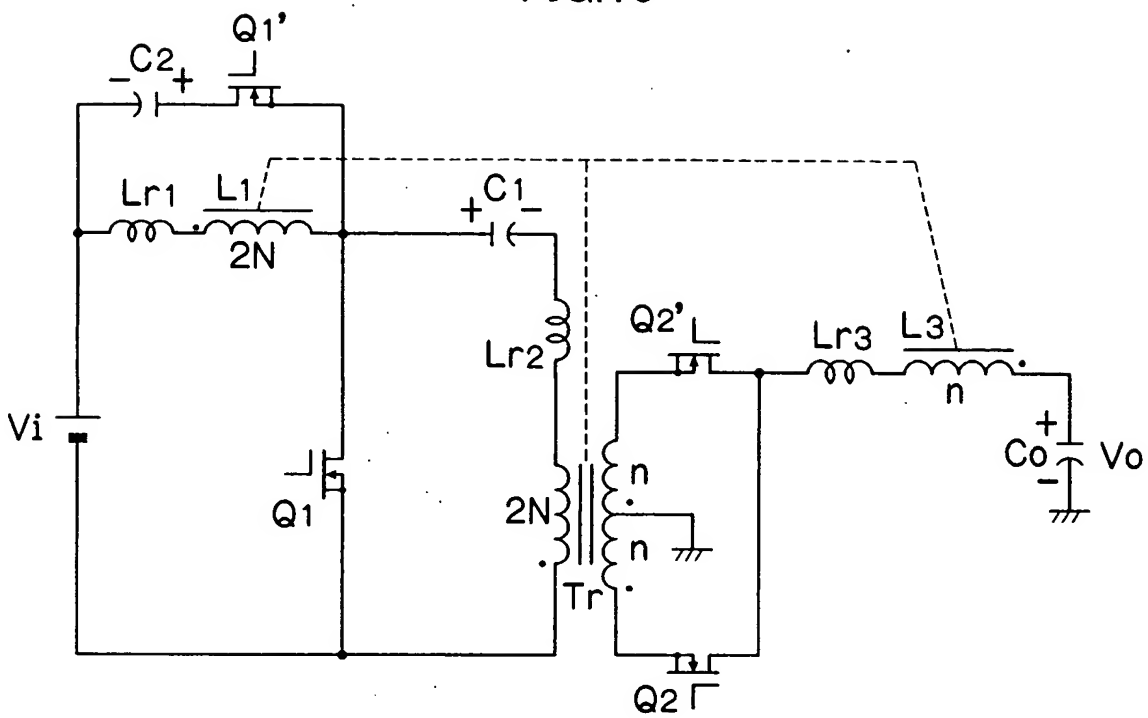

Q1'
C2
Lr1
L1
2N
C1
Lr2
Q2'
Lr3
L3
n
Vi
Co
Vo
Q1
2N
n
n
Tr
Q2

FIG.14

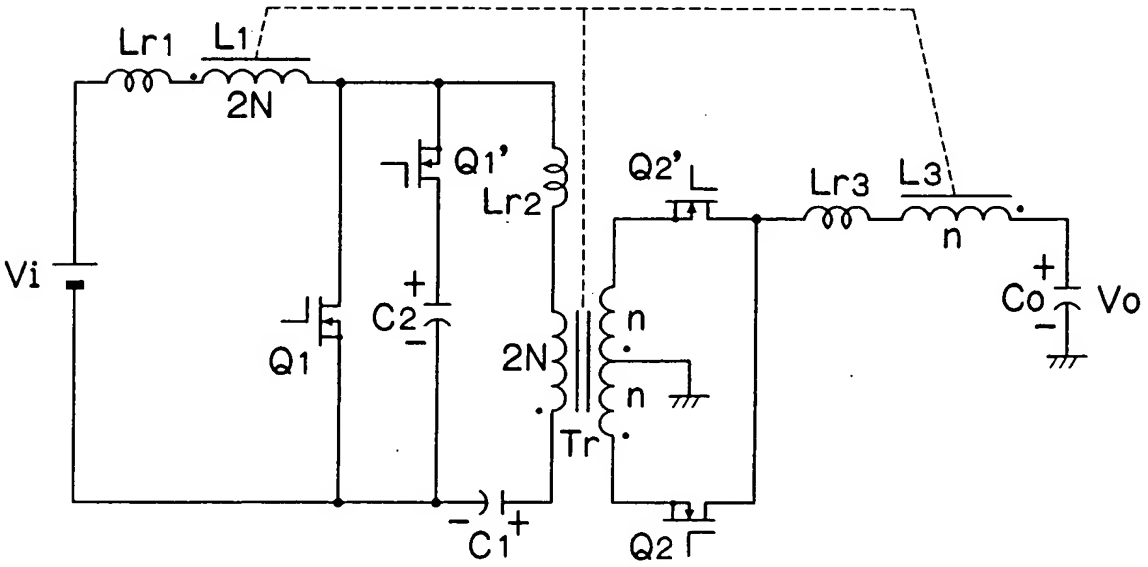

Lr1
L1
2N
Q1'
Lr2
Q2'
Lr3
L3
n
Vi
Co
Vo
C2
Q1
2N
n
n
Tr
C1
Q2

FIG.15

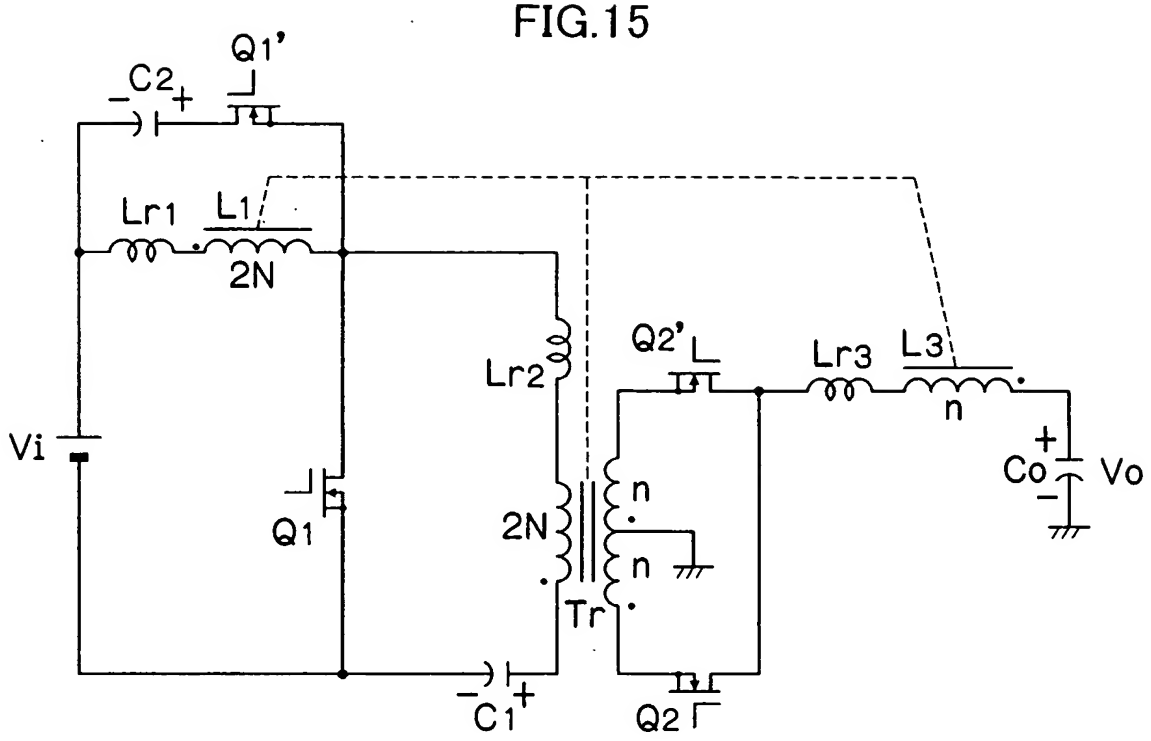

Q1'
C2
Lr1
L1
2N
Vi
Q1
Lr2
2N
Tr
n
n
Q2'
Lr3
L3
n
Co
Vo
C1
Q2

FIG.16

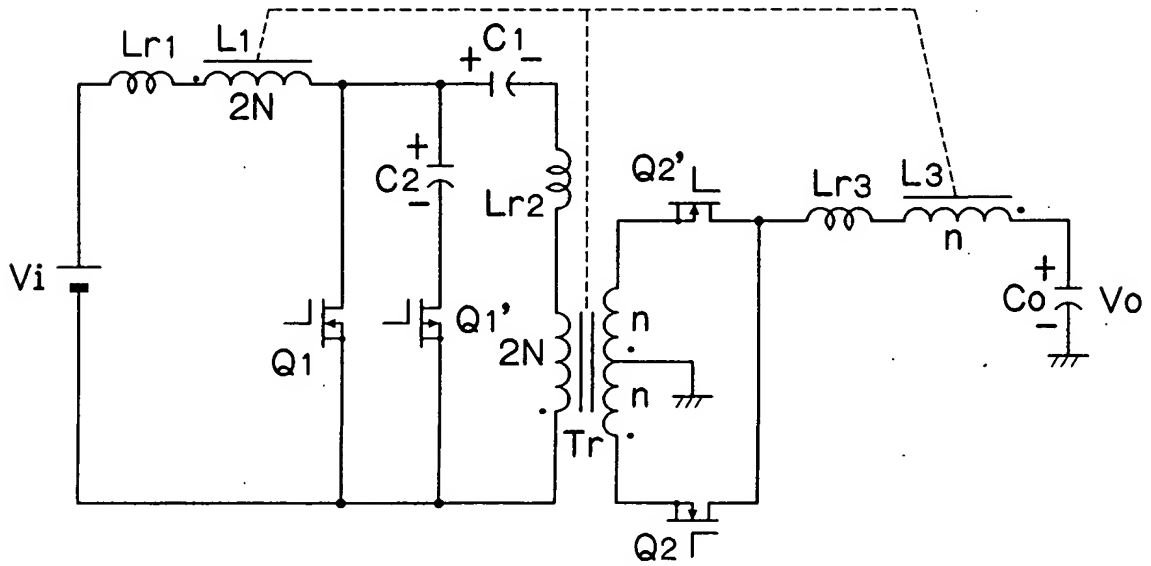

Lr1
L1
2N
C1
C2
Lr2
Q2'
Lr3
L3
n
Vi
Q1
Q1'
2N
Tr
n
n
Co
Vo
Q2

FIG.17

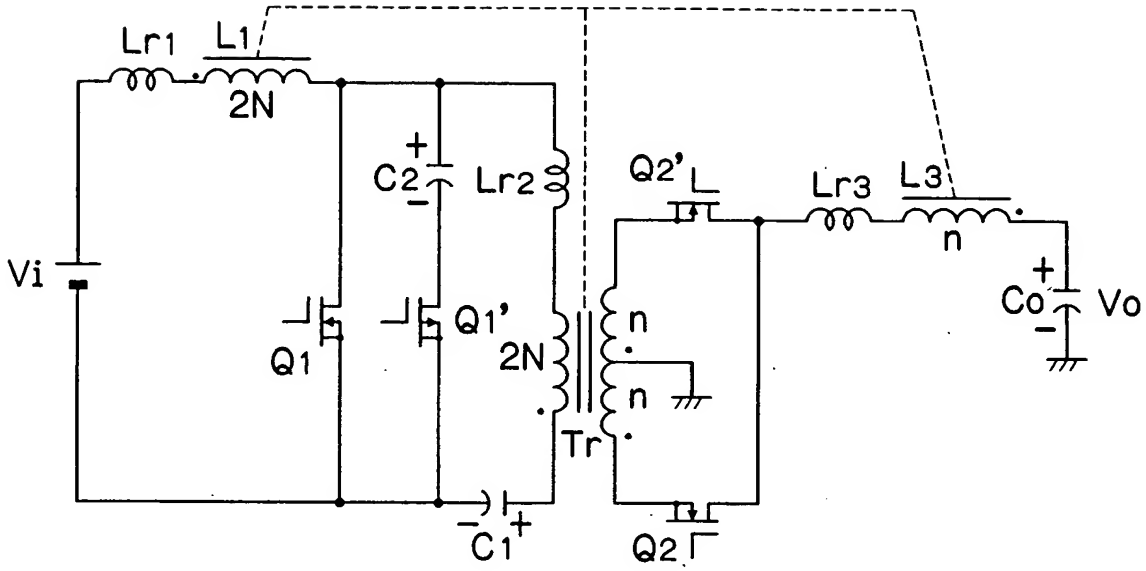

Lr1
L1
2N
C2
Lr2
Q2'
Lr3
L3
n
Vi
Co
Vo
Q1
Q1'
2N
n
n
Tr
C1
Q2

FIG.18

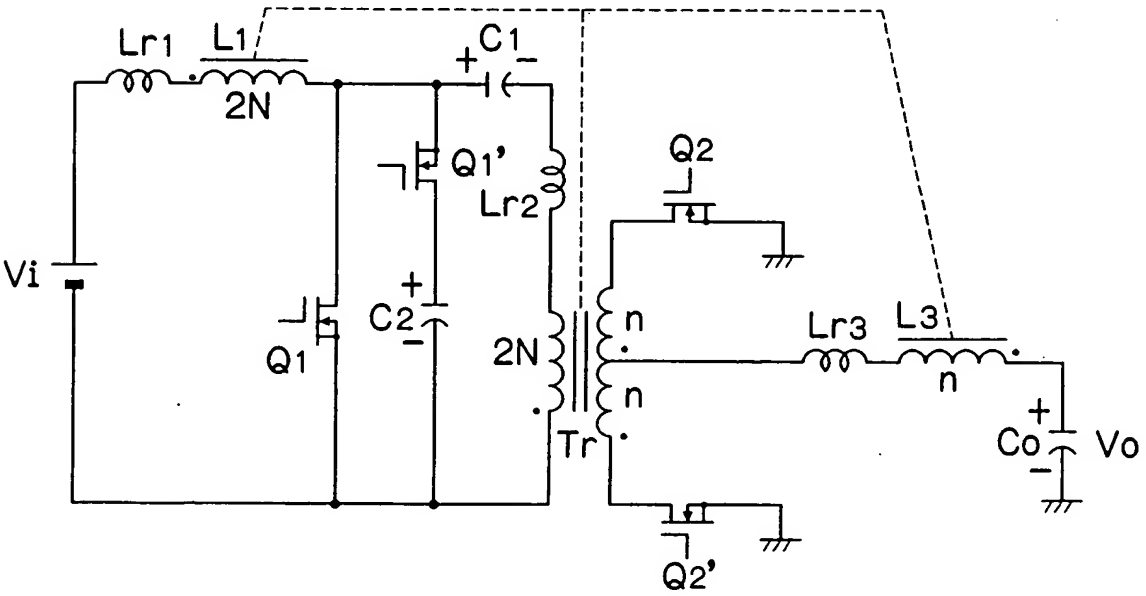

Lr1
L1
2N
C1
Q2
Q1'
Lr2
Vi
C2
n
Lr3
L3
Q1
2N
n
n
Co
Vo
Tr
Q2'

FIG.19

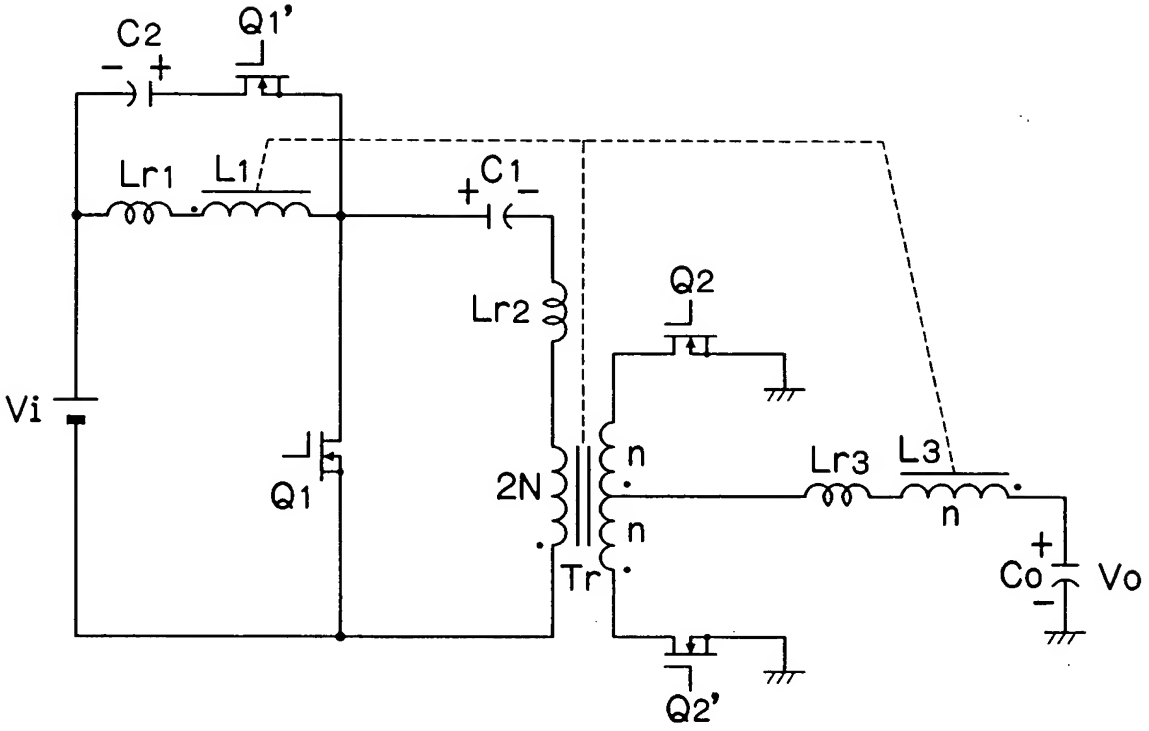

C2
Q1'
Lr1
L1
C1
Q2
Lr2
Vi
Q1
2N
n
n
Lr3
L3
n
Co
Vo
Tr
Q2'

FIG.20

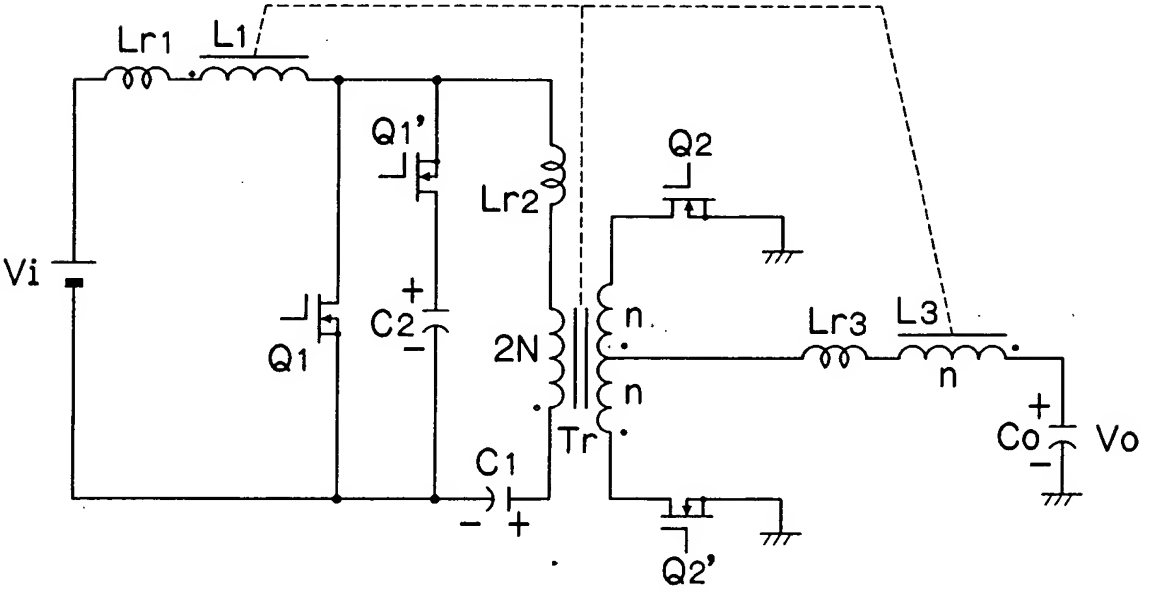

Lr1
L1
Q1'
Q2
Lr2
Vi
C2
Q1
2N
n
n
Lr3
L3
n
Co
Vo
Tr
C1
Q2'

FIG.21

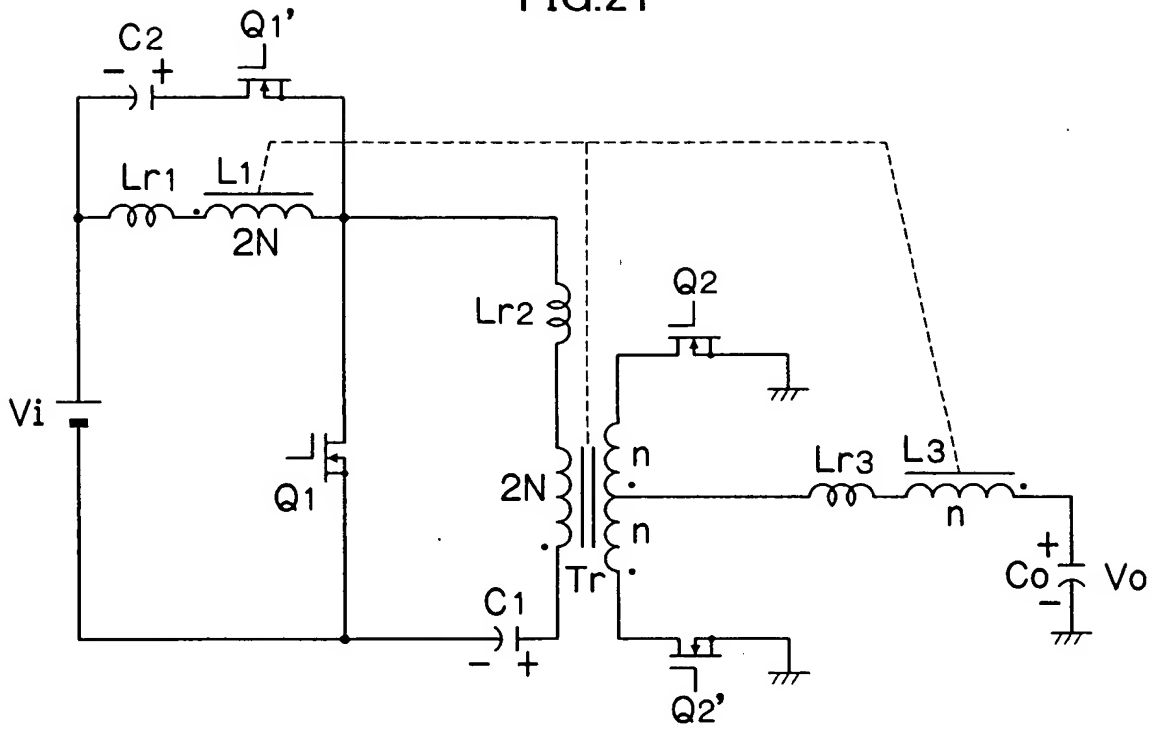

C2
Q1'
Lr1
L1
2N
Vi
Q1
Lr2
Q2
2N
n
n
Tr
Lr3
L3
n
Co
Vo
C1
Q2'

FIG.22

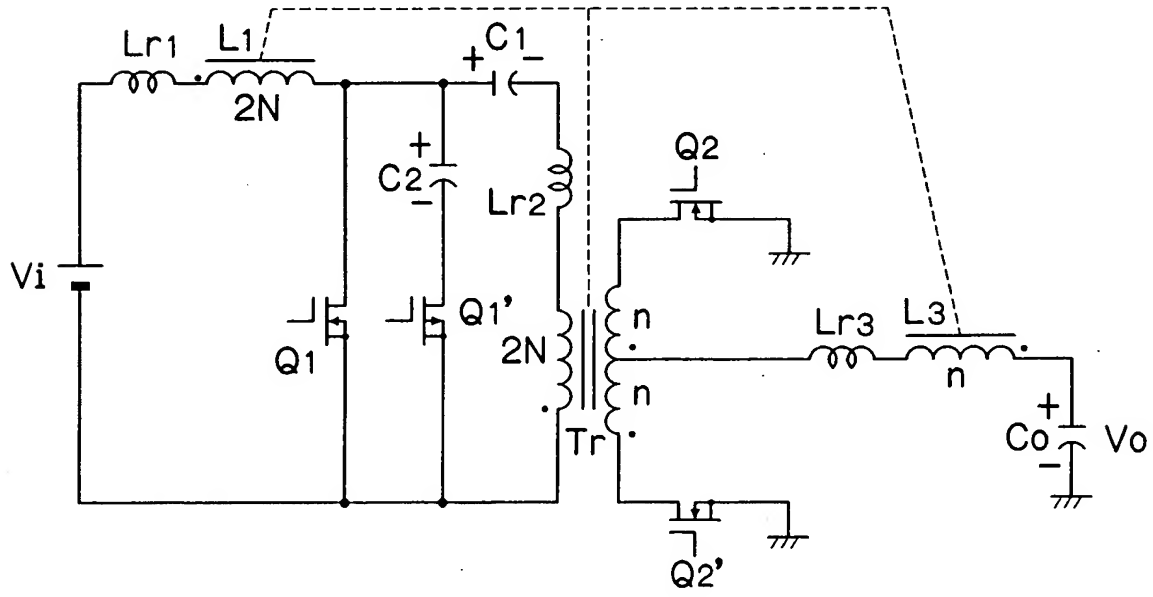

Lr1
L1
2N
C1
C2
Lr2
Q2
Vi
Q1
Q1'
2N
n
n
Tr
Lr3
L3
n
Co
Vo
Q2'

FIG.23

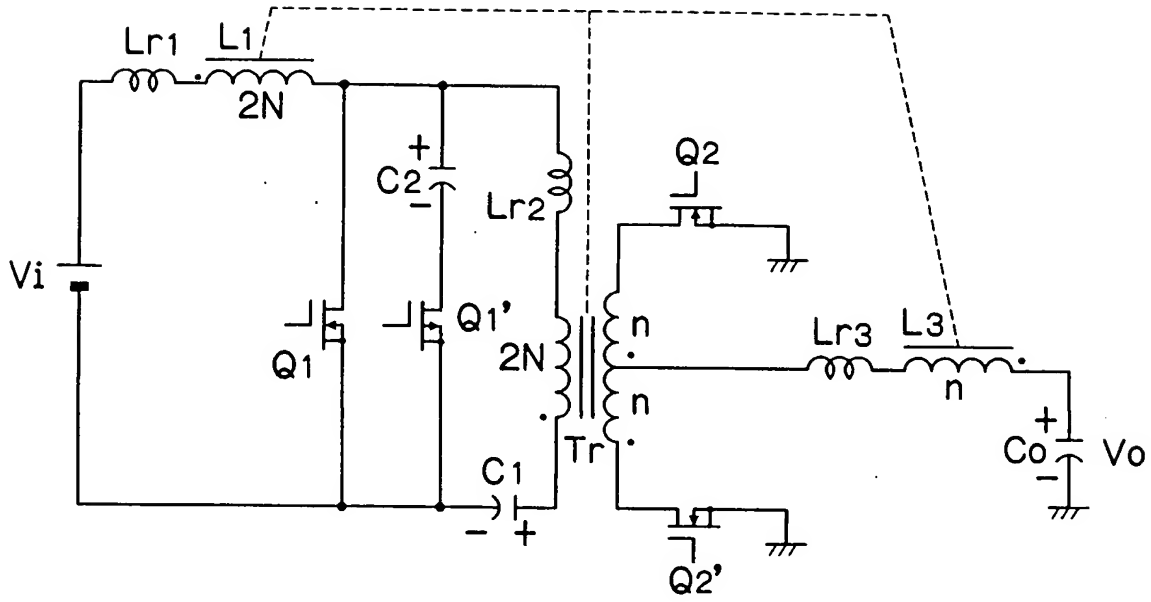
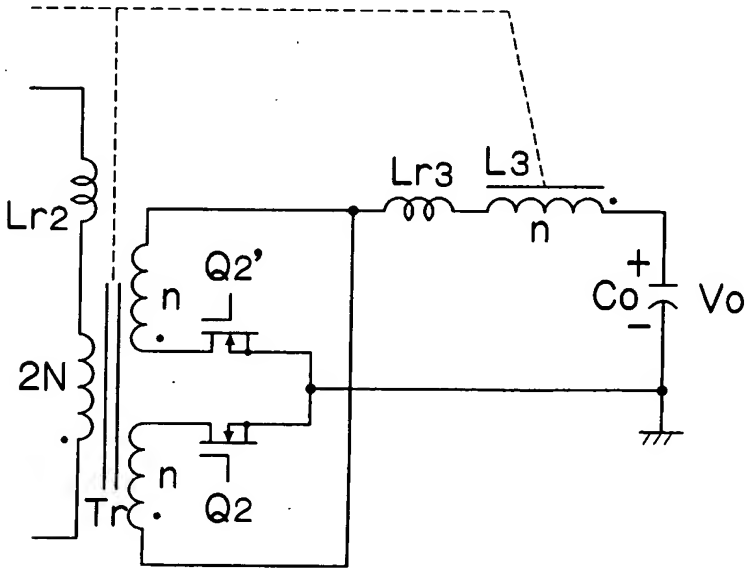
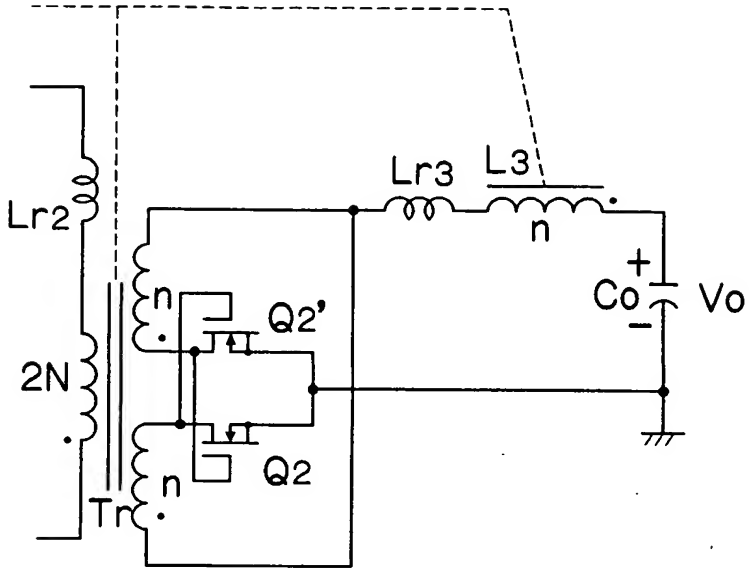


FIG.24



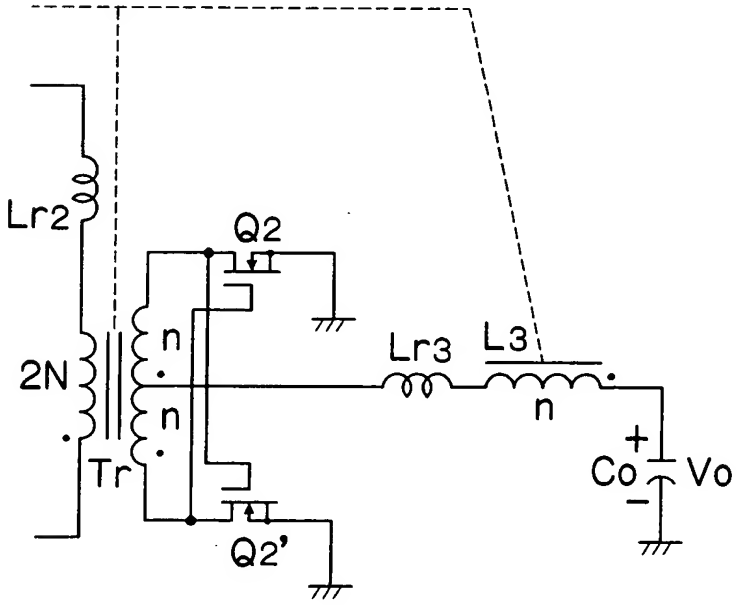
Tr PRIMARY CIRCUIT IS OMITTED

FIG.25



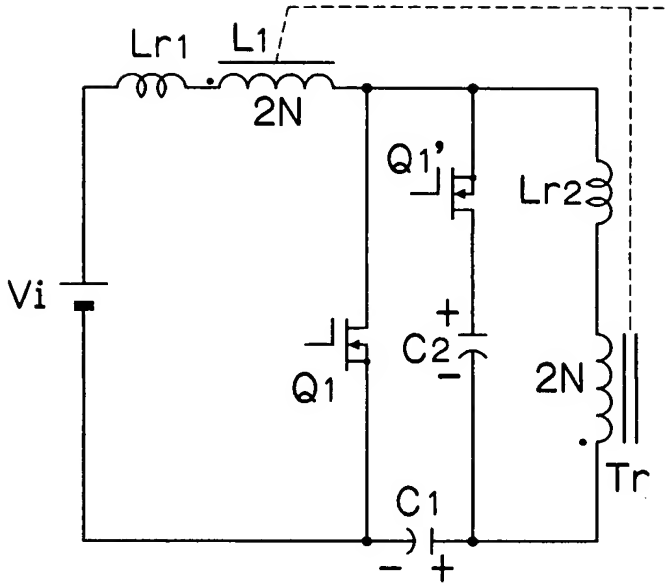
Tr PRIMARY CIRCUIT IS OMITTED

FIG.26



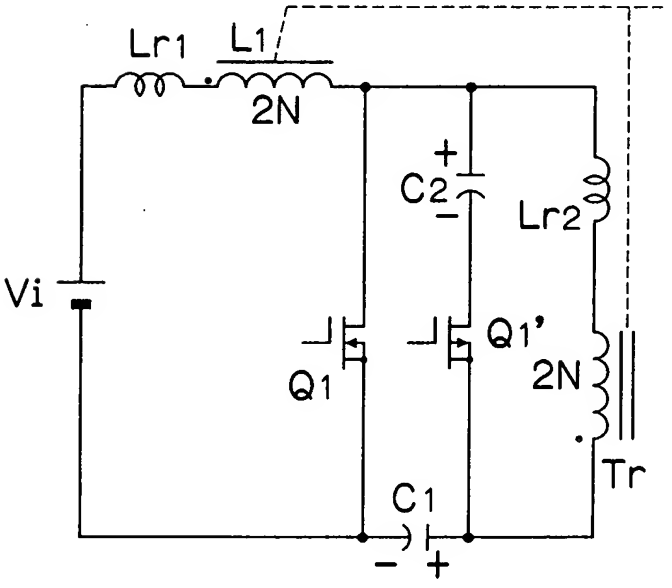
Tr PRIMARY CIRCUIT IS OMITTED

FIG.27



Tr SECONDARY CIRCUIT IS OMITTED

FIG.28



Tr SECONDARY CIRCUIT IS OMITTED

FIG.29
PRIOR ART